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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,874	09/22/2003	Minoru Okamoto	60188-657	4233

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,874	OKAMOTO, MINORU	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-5, in the Paper filed 08/12/04 is acknowledged. Applicant indicated a desire to cancel claims 6-11 in his remarks. However, under revised amendment practice 37 CFR 1.121 effective 7/30/2003, in order to cancel certain claims Applicant must supply a "marked up" copy of all claims indicating the cancelled claims "cancelled." Claims 6-11 have been withdrawn but not cancelled. Also in his remarks, Applicant correctly points out that claims 1-5 are device claims searchable in class 257.

Oath/Declaration

2. The oath/declaration filed on 22 September 2003 is acceptable.

Drawings

3. The formal drawings filed on 22 September 2003 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 22 September 2003 has been considered.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSUJI (5,901,023) in view of PARTOVI ET AL. (5,453,713).

Tsuji discloses a semiconductor integrated circuit device including a digital circuit 14,15 and an analog circuit 11, said device comprising a first (digital) electrostatic destruction protection circuit 50a (the two outboard ESD circuits 50a seen in figure 5B are the digital ESD circuits), connected to the digital circuit 14,15, for protecting the digital circuit 14,15 from destruction caused by ESD in the digital circuit 14,15 by an

influence of an input digital signal; and a second (analog) electrostatic destruction protection circuit 50a (the two inboard ESD circuits 50a seen in figure 5B are the analog ESD circuits), connected to the analog circuit 11, for protecting the analog circuit 11 from destruction caused by ESD in the analog circuit 11 by an influence of an input analog signal, first (digital) grounding conductors 19,21 connected to the first (digital) electrostatic destruction protection circuits 50a and a second (analog) grounding conductor 17 connected to the second (analog) electrostatic destruction protection circuit 50a wherein said first (digital) grounding conductor 19,21 and said second (analog) grounding conductor 17 are connected to each other via a member 30,31 for electrically connecting the semiconductor integrated circuit device to a package substrate of the semiconductor integrated circuit device, outside the semiconductor integrated circuit device. Note figures 5A and 5B and column 2 lines 14-37 of Tsuji.

Tsuji does not disclose that the digital circuit and the analog circuit are integrated on a single semiconductor chip.

However, Partovi et al. discloses means for providing a digital circuit and an analog circuit integrated on a single semiconductor chip by providing analog circuits 21A in an island 20 isolated from the digital circuitry that surrounds perimeter 21 on the single chip face. Note figure 1 and column 3 lines 10-32 of Partovi et al. Therefore, it would have been obvious to a person having skill in the art to modify Tsuji's semiconductor integrated circuit device by providing the digital circuit and the analog circuit integrated on a single semiconductor chip such as taught by Partovi et al. in order to combine

analog and digital functionality on a single chip without subjecting the analog circuit to an excessively noisy environment to thus provide a more compact and cheaply built analog/digital device.

With regard to claims 2 and 3, although neither Tsuji nor Partovi et al. teach that the first (digital) grounding conductor and the second (analog) grounding conductor are connected to each other inside (as required by claim 2) or outside (as required by claim 3) a package substrate of the semiconductor integrated circuit device, the differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
09/04

Minhloan Tran
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